DiePak®
Known Good Die Solutions

Die Carrier
Temporary Reusable Packages




AEHR TEST SYSTEMS

Setting the Standards for Tomorrow

Die Level Burn-in and Test

The Need for KGD

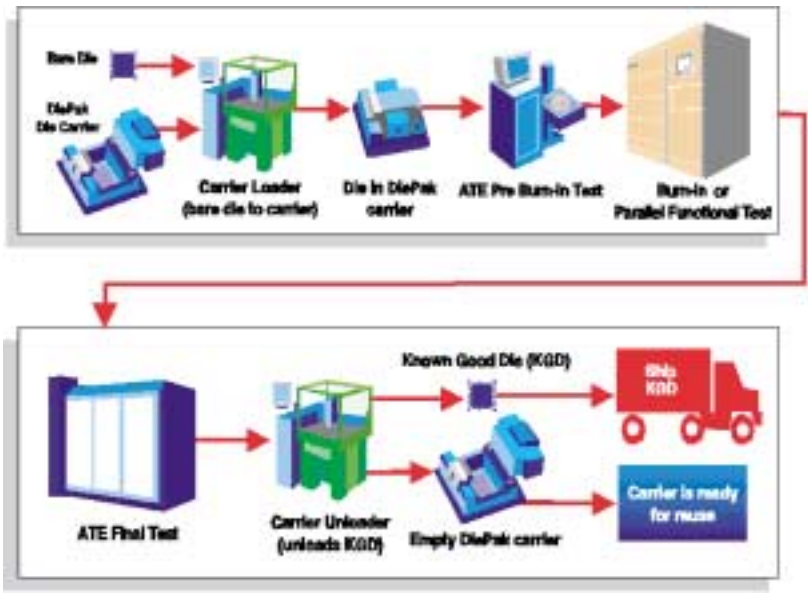
Historically, semiconductor manufacturers and end-users performed numerous tests on packaged devices to help assure product reliability. More recently, both suppliers and customers identified the value of performing die-level electrical tests at speed and temperature.

More and more IC manufacturers are assembling die into expensive Memory Modules, Multi-Chip-Modules (MCMs), and Chip On-Board (COB) packages to increase product capabilities. Unfortunately, when they detect failures in these packages, they must undertake a time-consuming repair process to isolate and replace the failed die–often at high cost.

Reducing Production Costs

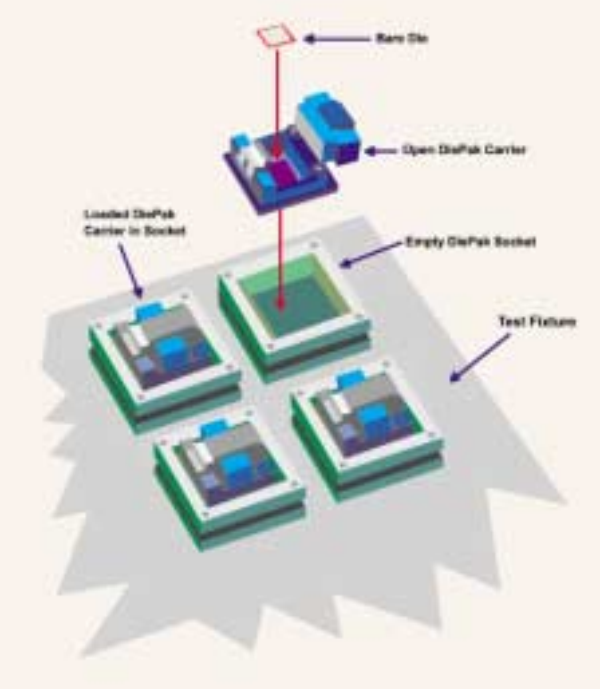
If your goal is to produce quality-assured bare die and control ever increasing testing and production costs, die-level burn-in and electrical testing can help reduce product packaging waste and production cost, and provide the ability to enter the bare die market.

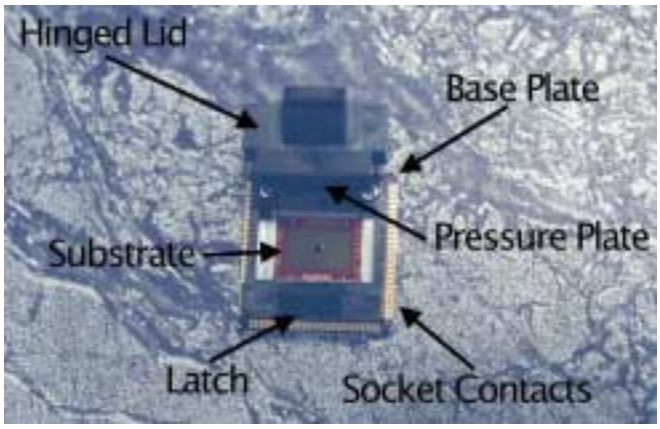
Effective development of Known Good Die (KGD) requires a solution that is cost competitive with current burn-in and test methods for packaged products. Aehr Test Systems has developed a complete testing process for handling, burning-in, and testing die using inexpensive, reusable die carriers. DiePak® is the industry leading solution.



DiePak Components

DiePak components include a temporary, reusable die carrier, an interconnect substrate, and burn-in sockets. This die interconnect and carrier system provides excellent low contact resistance.



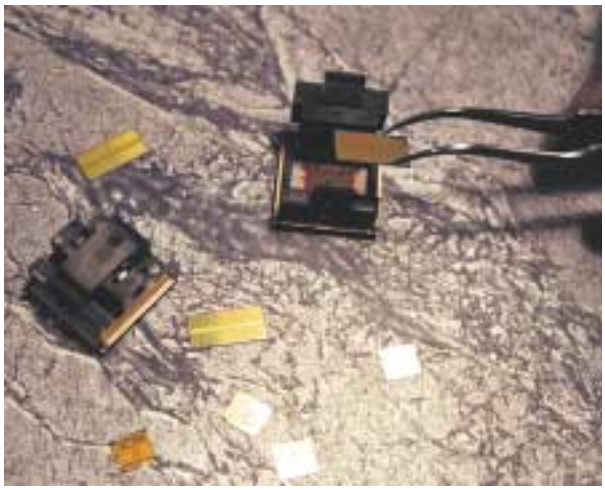


The Interconnect Substrate

The interconnect substrate provides electrical connection between the die pads and the burn-in socket contacts. A proprietary substrate material serves as the electrical interconnect. The substrate material is a polyimide film with fine line pitch copper traces and thru-holes filled with metal. This forms electrically conductive bumps on the polyimide surface of the film. The interconnect substrate can be designed for die with pads or solder bumps, and for both peripheral and array pads.

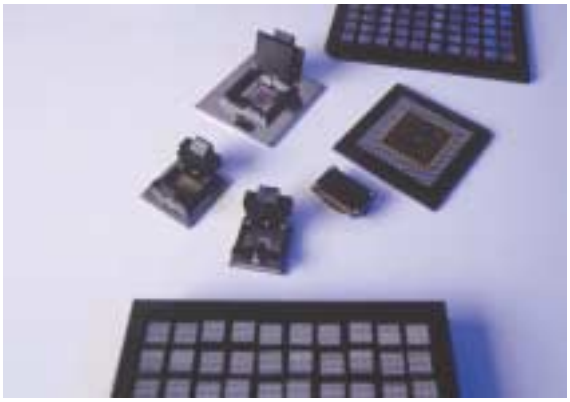
The DiePak Carrier

The DiePak carrier base provides the mechanical support for the substrate and the mechanical interface to the socket. The carrier contains an optional alignment mechanism that can safely and accurately align the die, substrate, and socket interface. When the carrier lid is closed, it applies a controlled force to the die for proper mating to the substrate. This also protects the die. The carrier provides the appropriate thermal mass to remove heat from the die. The DiePak design provides for automated, fast, and simple assembly of the die into the DiePak carrier and insertion into a burn-in board.



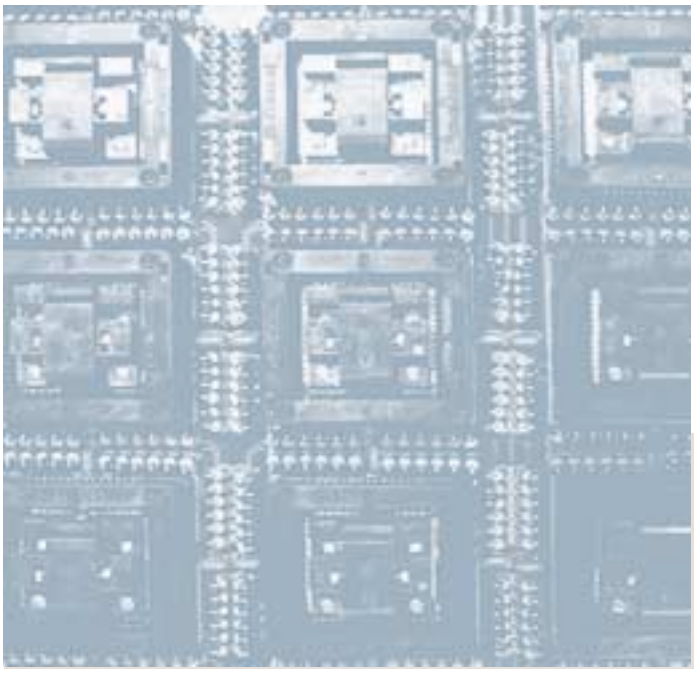
A Family of Carriers

The current DiePak product line includes a family of carriers that can accommodate die with various pin counts. This family of carriers reduces your cost by offering a standard design for a range of pin counts with custom interconnect substrates for different device types. With this standardized design you can use a universal burn-in board design and reduce the number of burn-in boards in your inventory.



The Socket

The DiePak solution includes a mating socket for each family of carriers. These sockets have a unique contact pin interface, resulting in a small socket footprint for high socket density on each burn-in board.



Advantages of the DiePak Solution

- Rated "Best Performer" by MCC industry-wide evaluation of KGD carriers
- Use the same carrier for pre burn-in ATE, burn-in, and post burn-in electrical testing
- Once a bare die is inserted into the DiePak carrier, it is protected from handling damage
- DiePak carrier loading and handling is easily automated
- Smallest footprint in the industry: This means you can have a more populated burn-in board, so you burn-in more die with fewer burn-in boards and test more devices in parallel
- Use for Wire-bond die, Flip-chip, and Chip-scale packages--for memory, microcontrollers, ASICs, and microprocessors
- Lowest cost of ownership in the market
- You can use DiePak with your existing ATE, handling, and burn-in systems. You don't have to retool your test floor to use DiePak carriers

DiePak Carrier Family

Pin Count	Maximum Die Size	Pin Pitch
66	335 mil X 629 mil (8.5mm X 16mm)	19.68 mil (0.500mm)
56/108	345 mil X 575 mil (8.8mm X 14.6mm)	25.00 mil (0.635mm)
172	345 mil X 575 mil (8.8mm X 14.6mm)	19.68 mil (0.500mm)
320	750 mil X 750 mil (19.4mm X 19.4mm)	19.68 mil (0.500mm)

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